Abstract

Embodiments include a semiconductor device having a non-volatile memory transistor, the semiconductor device including a plurality of field effect transistors operated at a plurality of different voltage levels. The semiconductor device has a memory region 4000, and first, second and third transistor regions 1000, 2000 and 3000 respectively including field effect transistors that operate at different voltage levels. The memory region 4000 includes a split-gate non-volatile memory transistor 400. The first transistor region 1000 includes a first voltage-type transistor 100 that operates at a first voltage level. The second transistor region 2000 includes a second voltage-type transistor 200 that operates at a second voltage level. The third transistor region 3000 includes a third voltage-type transistor that operates at a third voltage level. The second voltage-type transistor 200 has a gate insulation layer 22 that is formed from at least two insulation layers 22a and 22b. The insulation layer 22b is formed in the same step in which a gate insulation layer 20 of the first voltage-type transistor 100 is formed.